FIG. 1

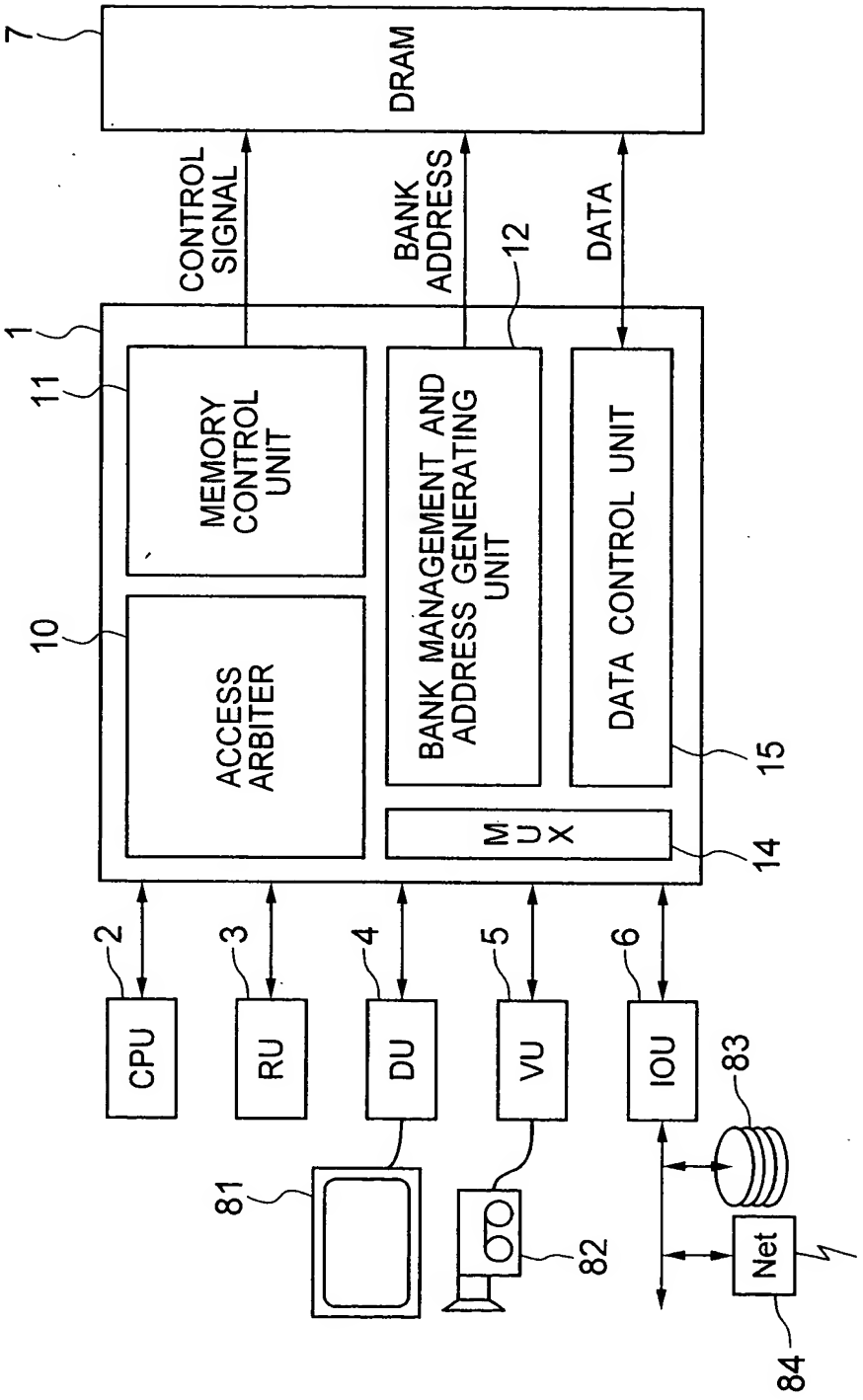

7
DRAM
CONTROL SIGNAL
BANK ADDRESS
12
DATA
1
11
MEMORY CONTROL UNIT
10
ACCESS ARBITER
BANK MANAGEMENT AND ADDRESS GENERATING UNIT
DATA CONTROL UNIT
15
MUX
14
2
3
4
5
6
CPU
RU
DU
VU
IOU
83
81
82
Net
84

FIG. 2

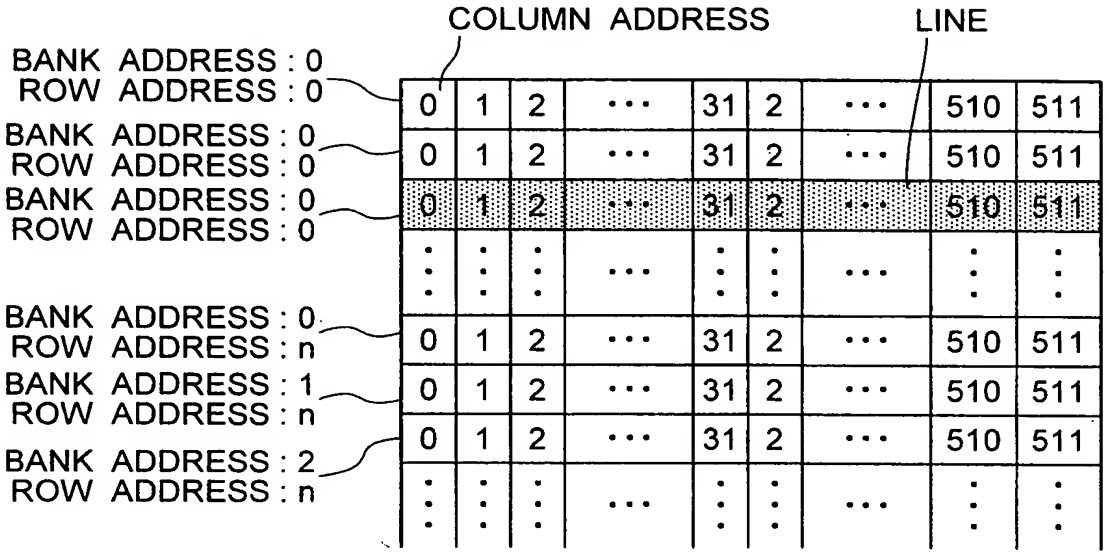

COLUMN ADDRESS
LINE
BANK ADDRESS : 0
ROW ADDRESS : 0
BANK ADDRESS : 0
ROW ADDRESS : 0
BANK ADDRESS : 0
ROW ADDRESS : 0
BANK ADDRESS : 0
ROW ADDRESS : n
BANK ADDRESS : 1
ROW ADDRESS : n
BANK ADDRESS : 2
ROW ADDRESS : n
0 1 2 ··· 31 2 ··· 510 511

FIG. 3

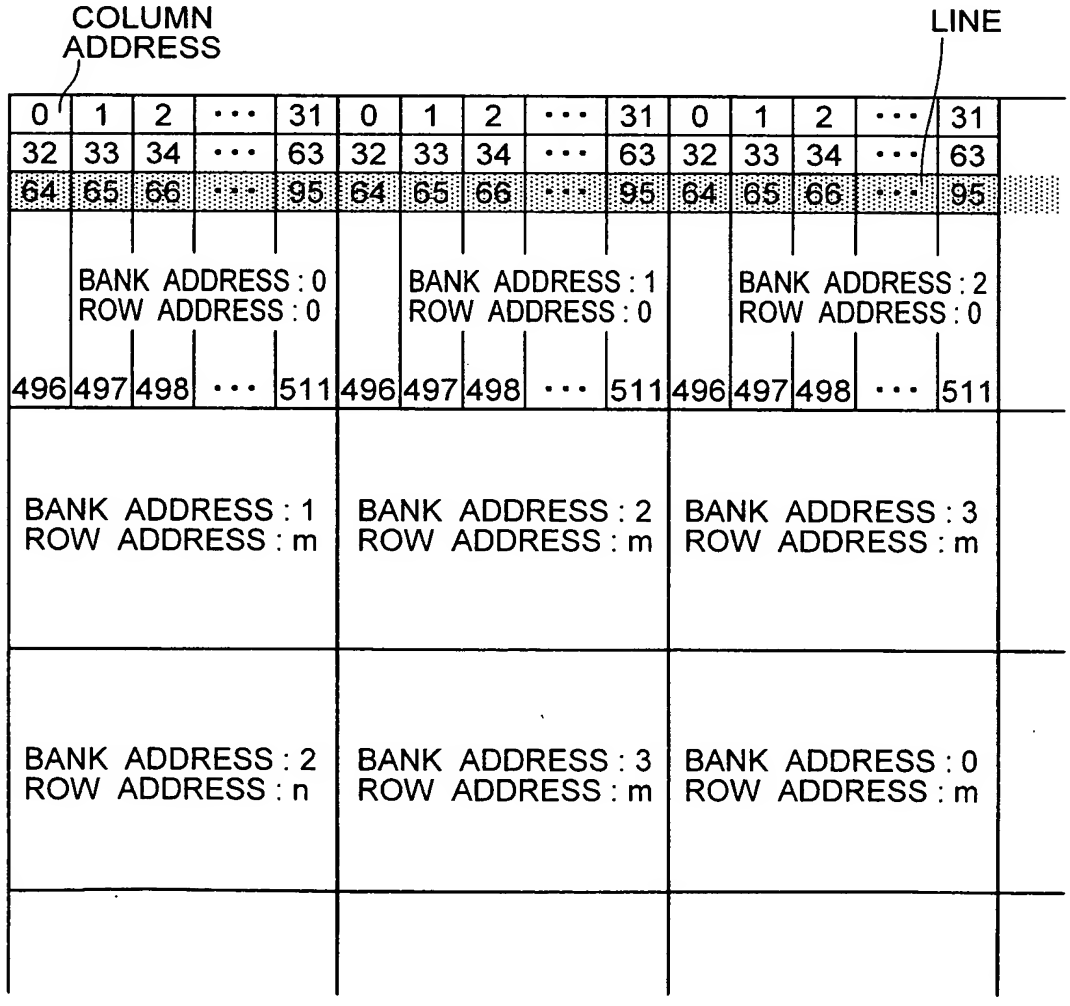

COLUMN ADDRESS
LINE
0 1 2 ··· 31 0 1 2 ··· 31 0 1 2 ··· 31
32 33 34 ··· 63 32 33 34 ··· 63 32 33 34 ··· 63
64 65 66 ··· 95 64 65 66 ··· 95 64 65 66 ··· 95
BANK ADDRESS : 0
ROW ADDRESS : 0
BANK ADDRESS : 1
ROW ADDRESS : 0
BANK ADDRESS : 2
ROW ADDRESS : 0
496 497 498 ··· 511 496 497 498 ··· 511 496 497 498 ··· 511
BANK ADDRESS : 1
ROW ADDRESS : m
BANK ADDRESS : 2
ROW ADDRESS : m
BANK ADDRESS : 3
ROW ADDRESS : m
BANK ADDRESS : 2
ROW ADDRESS : n
BANK ADDRESS : 3
ROW ADDRESS : m
BANK ADDRESS : 0
ROW ADDRESS : m

FIG. 4

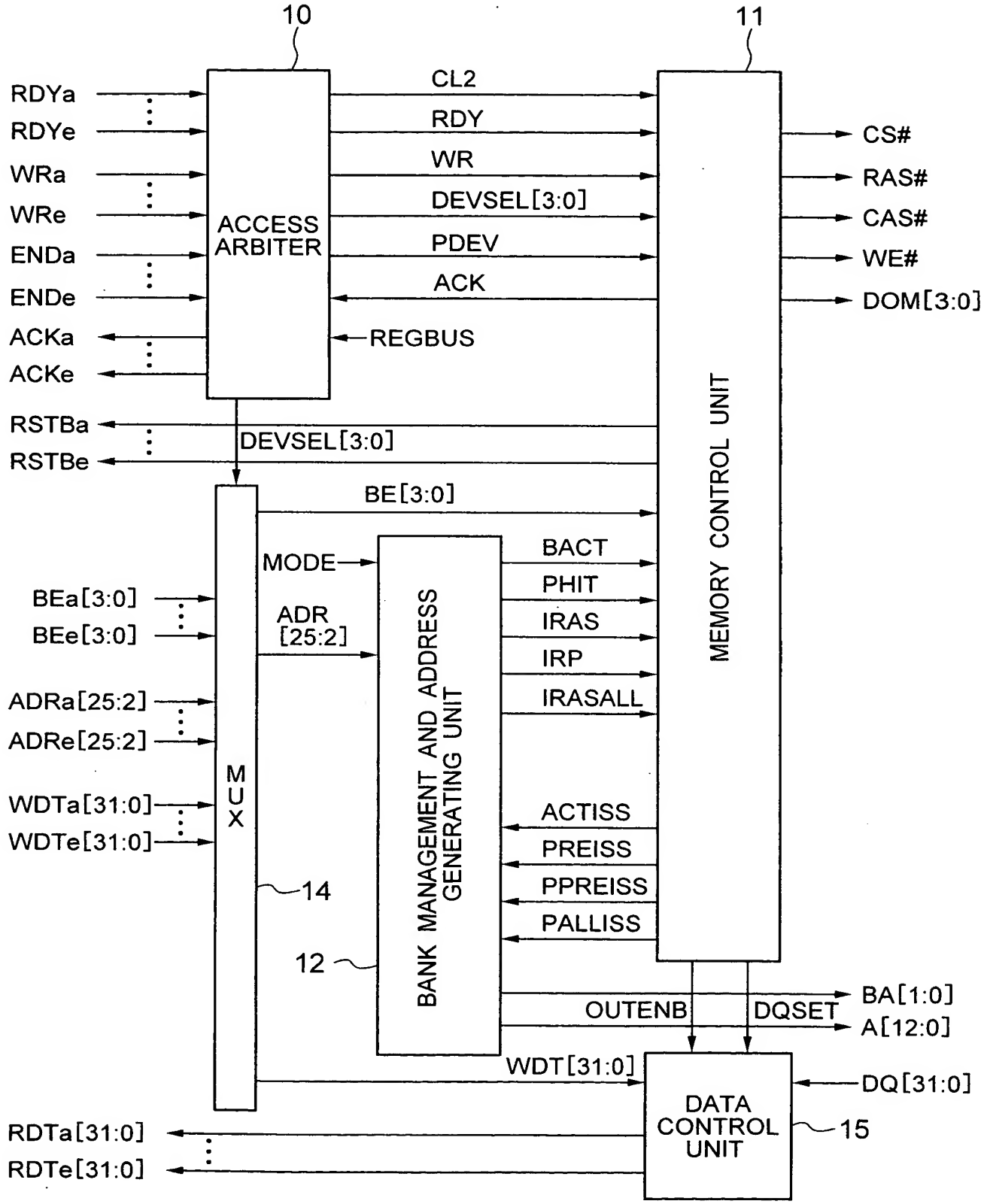

10
11
RDYa
RDYe
WRa
WRe
ENDa
ENDe
ACKa
ACKe
ACCESS ARBITER
CL2
RDY
WR
DEVSEL[3:0]
PDEV
ACK
REGBUS
RSTBa
RSTBe
DEVSEL[3:0]
MEMORY CONTROL UNIT
CS#
RAS#
CAS#
WE#
DOM[3:0]
BE[3:0]
MODE
ADR [25:2]
BEa[3:0]
BEe[3:0]
ADRa[25:2]
ADRe[25:2]
WDTa[31:0]
WDTe[31:0]
MUX
14
12
BANK MANAGEMENT AND ADDRESS GENERATING UNIT
BACT
PHIT
IRAS
IRP
IRASALL
ACTISS
PREISS
PPREISS
PALLISS
BA[1:0]
A[12:0]
OUTENB
DQSET
WDT[31:0]
DQ[31:0]
DATA CONTROL UNIT
15
RDTa[31:0]
RDTe[31:0]

FIG. 5

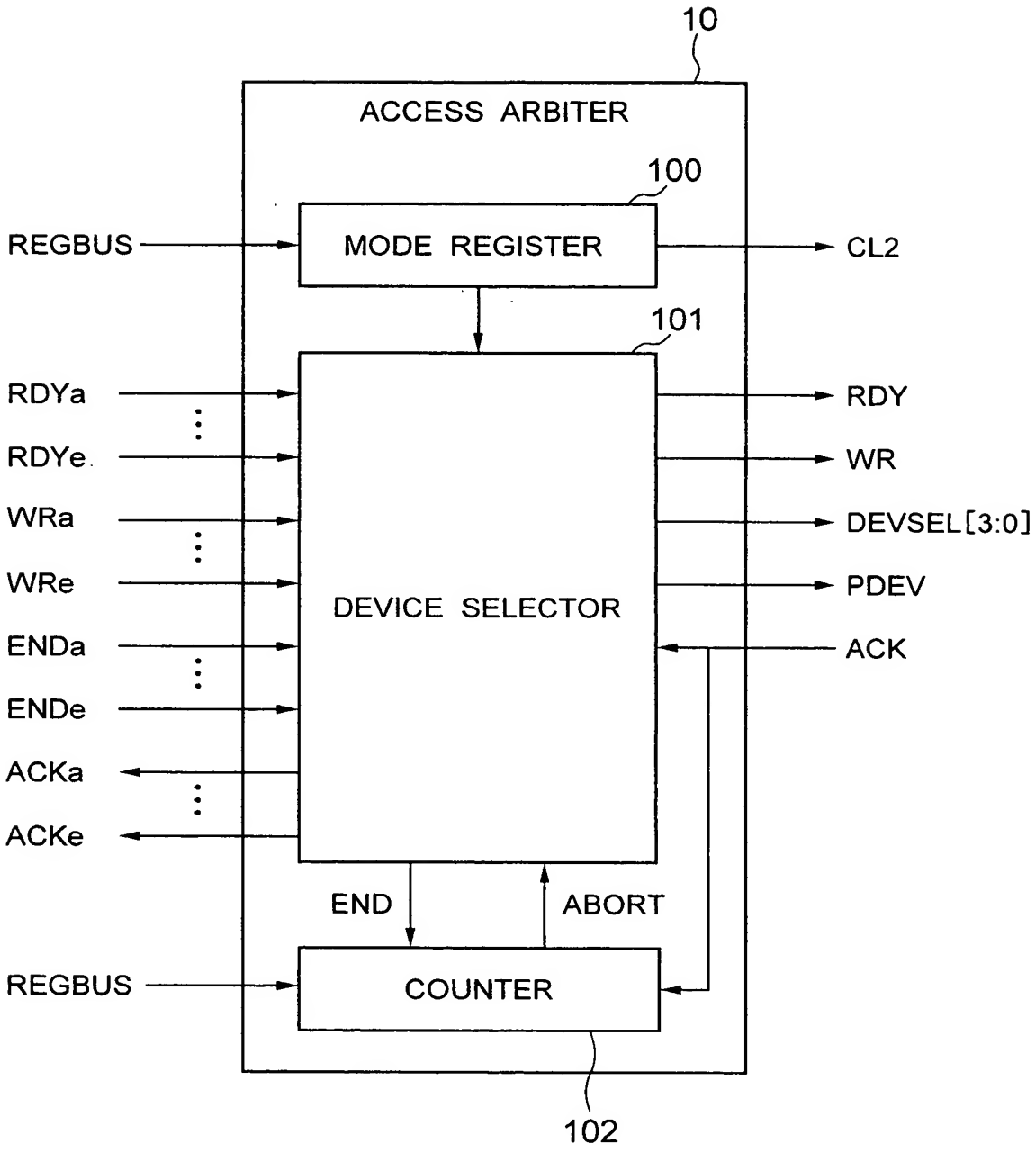

10
ACCESS ARBITER
100
MODE REGISTER
REGBUS
CL2
101
RDYa
RDYe
WRa
WRe
ENDa
ENDe
ACKa
ACKe
DEVICE SELECTOR
RDY
WR
DEVSEL[3:0]
PDEV
ACK
END
ABORT
REGBUS
COUNTER
102

FIG. 6

MODE REGISTER	PRa[2:0]	PRb[2:0]	PRc[2:0]	PRd[2:0]	PRe[2:0]	CL2	PDa	PDb	PDc	PDd	PDe
SETTING EXAMPLE :	000	001	010	011	010	1	0	1	0	0	1

FIG. 7

PRi[2:0]	PRIORITY
000	PRIVILEGE MODE
001	PRIORITY : HIGH
010	
011	
100	
101	
110	
111	PRIORITY : LOW

FIG. 8

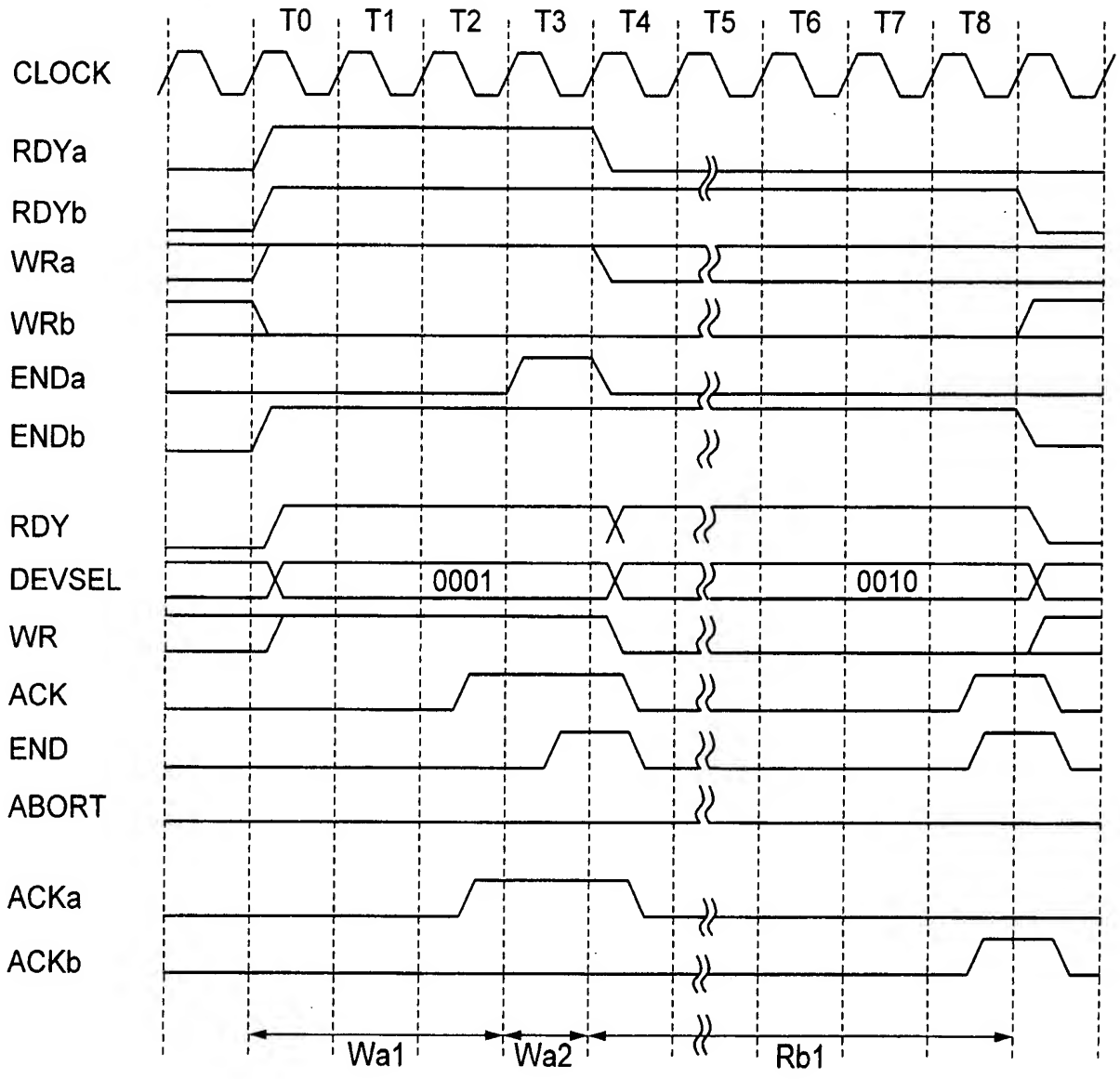

T0
T1
T2
T3
T4
T5
T6
T7
T8
CLOCK
RDYa
RDYb
WRa
WRb
ENDa
ENDb
RDY
DEVSEL
0001
0010
WR
ACK
END
ABORT
ACKa
ACKb
Wa1
Wa2
Rb1

FIG. 9

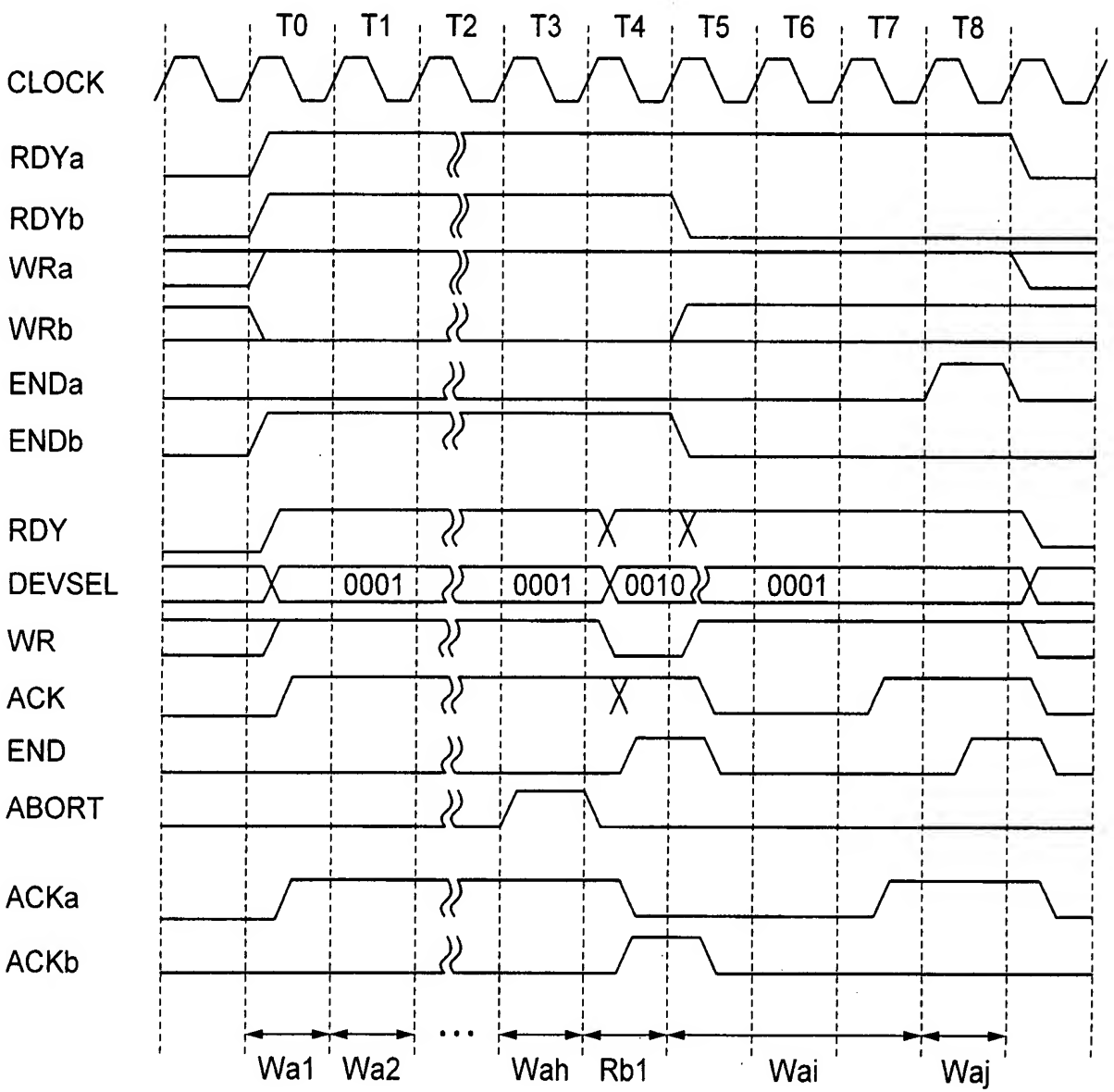

T0
T1
T2
T3
T4
T5
T6
T7
T8
CLOCK
RDYa
RDYb
WRa
WRb
ENDa
ENDb
RDY
DEVSEL
0001
0001
0010
0001
WR
ACK
END
ABORT
ACKa
ACKb
Wa1
Wa2
Wah
Rb1
Wai
Waj

FIG. 10

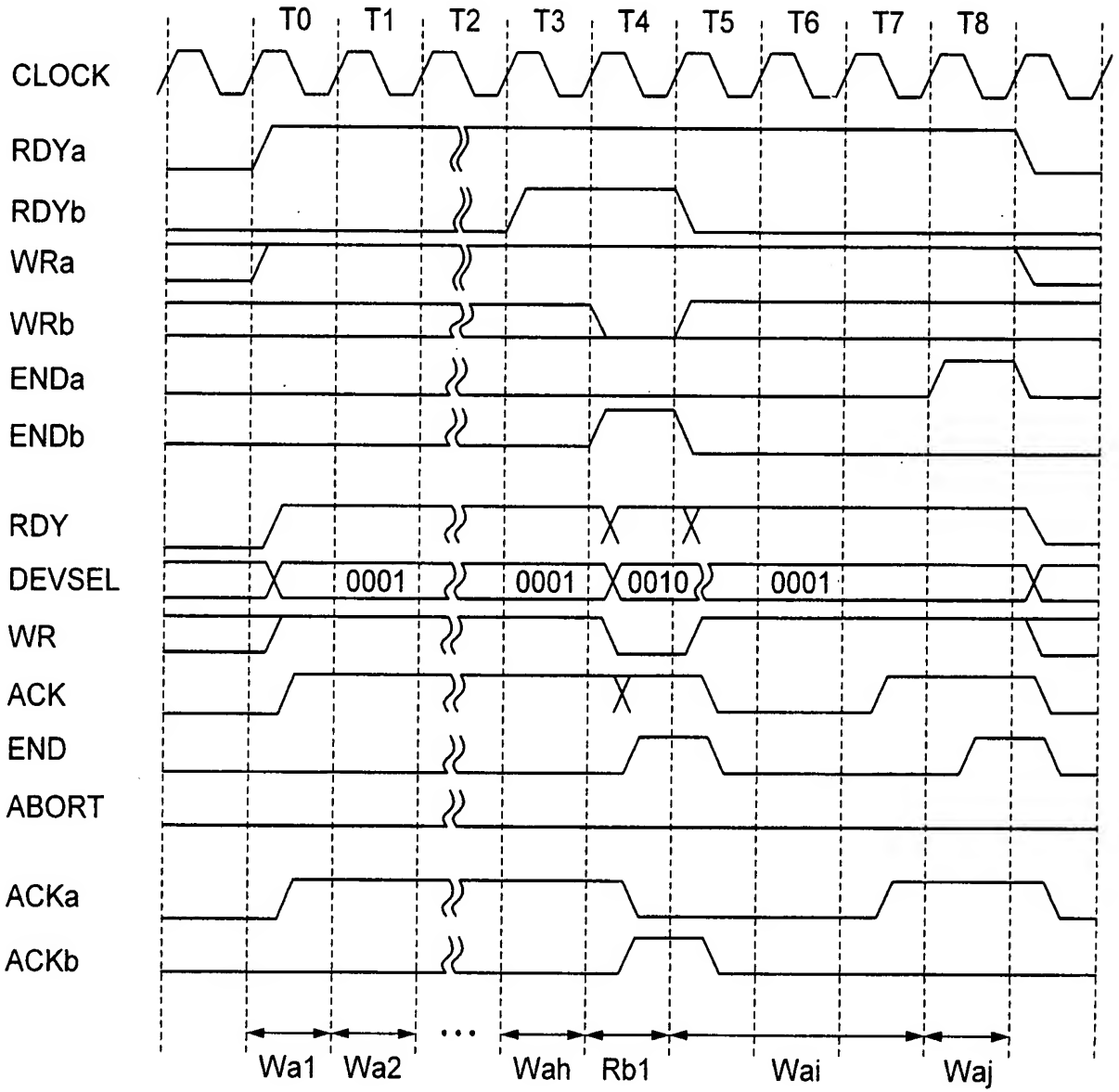

T0
T1
T2
T3
T4
T5
T6
T7
T8
CLOCK
RDYa
RDYb
WRa
WRb
ENDa
ENDb
RDY
DEVSEL
0001
0001
0010
0001
WR
ACK
END
ABORT
ACKa
ACKb
Wa1
Wa2
Wah
Rb1
Wai
Waj

FIG. 11

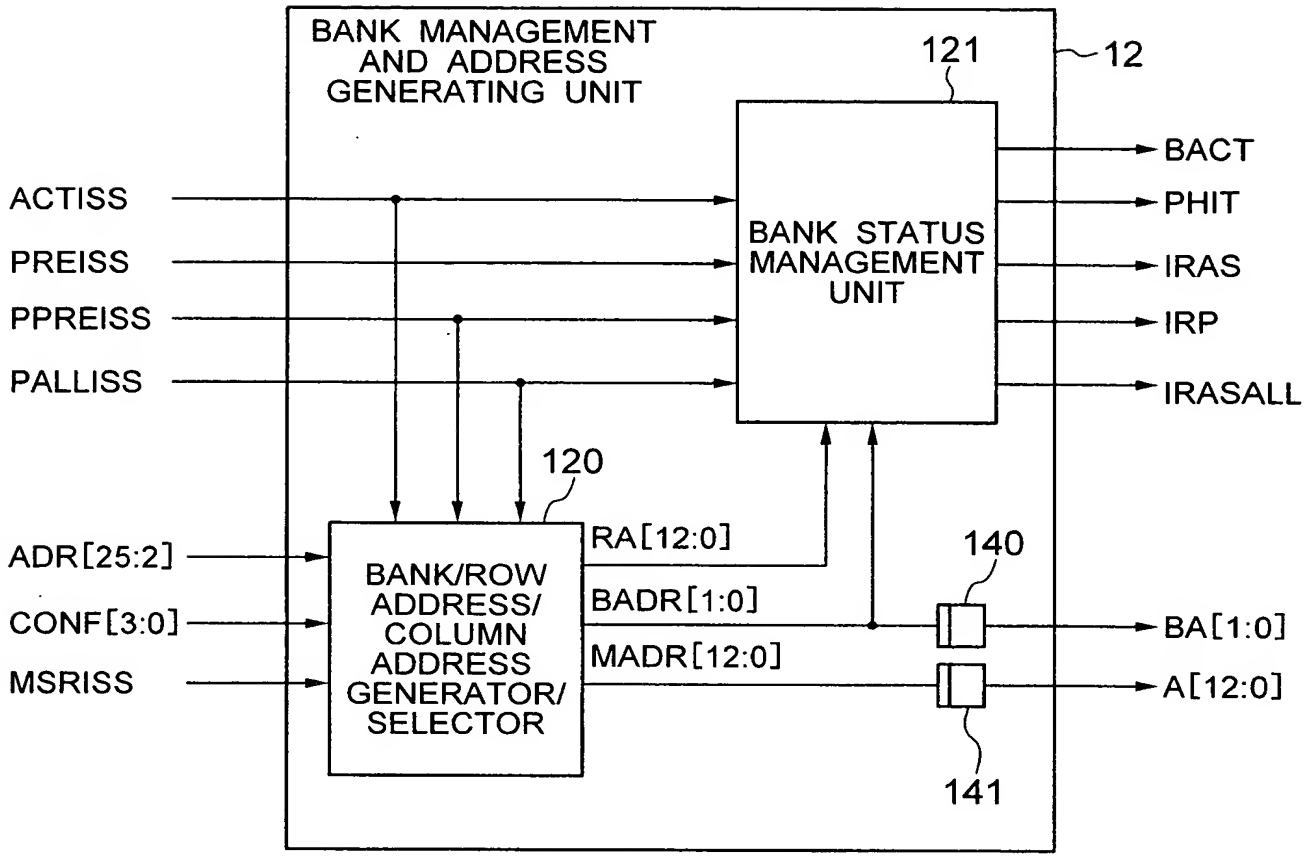

BANK MANAGEMENT AND ADDRESS GENERATING UNIT
121
12
BANK STATUS MANAGEMENT UNIT
ACTISS
PREISS
PPREISS
PALLISS
BACT
PHIT
IRAS
IRP
IRASALL
120
ADR[25:2]
CONF[3:0]
MSRISS
BANK/ROW ADDRESS/ COLUMN ADDRESS GENERATOR/ SELECTOR
RA[12:0]
BADR[1:0]
MADR[12:0]
140
BA[1:0]
A[12:0]
141

FIG. 12

CONF [3:0]	ACTISS	PPREISS	PALLISS	BADR[1:0]	RA[12:0]	MADR[12:0]
0	0	0	0	ADR[11:10]	{0, ADR[23:12]}	{00000, ADR[9:2]}
	1	0	0			{0, ADR[23:12]}
	0	1	0	ADR[11:10]+1		{00000, ADR[9:2]}
	0	0	1	ADR[11:10]		{00100, ADR[9:2]}
1	0	0	0	ADR[12:11]	{0, ADR[24:13]}	{0000, ADR[10:2]}
	1	0	0			{0, ADR[23:12]}
	0	1	0	ADR[12:11]+1		{0000, ADR[10:2]}
	0	0	1	ADR[12:11]		{0010, ADR[10:2]}
2	0	0	0	ADR[12:11]	ADR[25:13]	{0000, ADR[10:2]}
	1	0	0			{0, ADR[23:12]}
	0	1	0	ADR[12:11]+1		{0000, ADR[10:2]}
	0	0	1	ADR[12:11]		{0010, ADR[10:2]}

FIG. 13

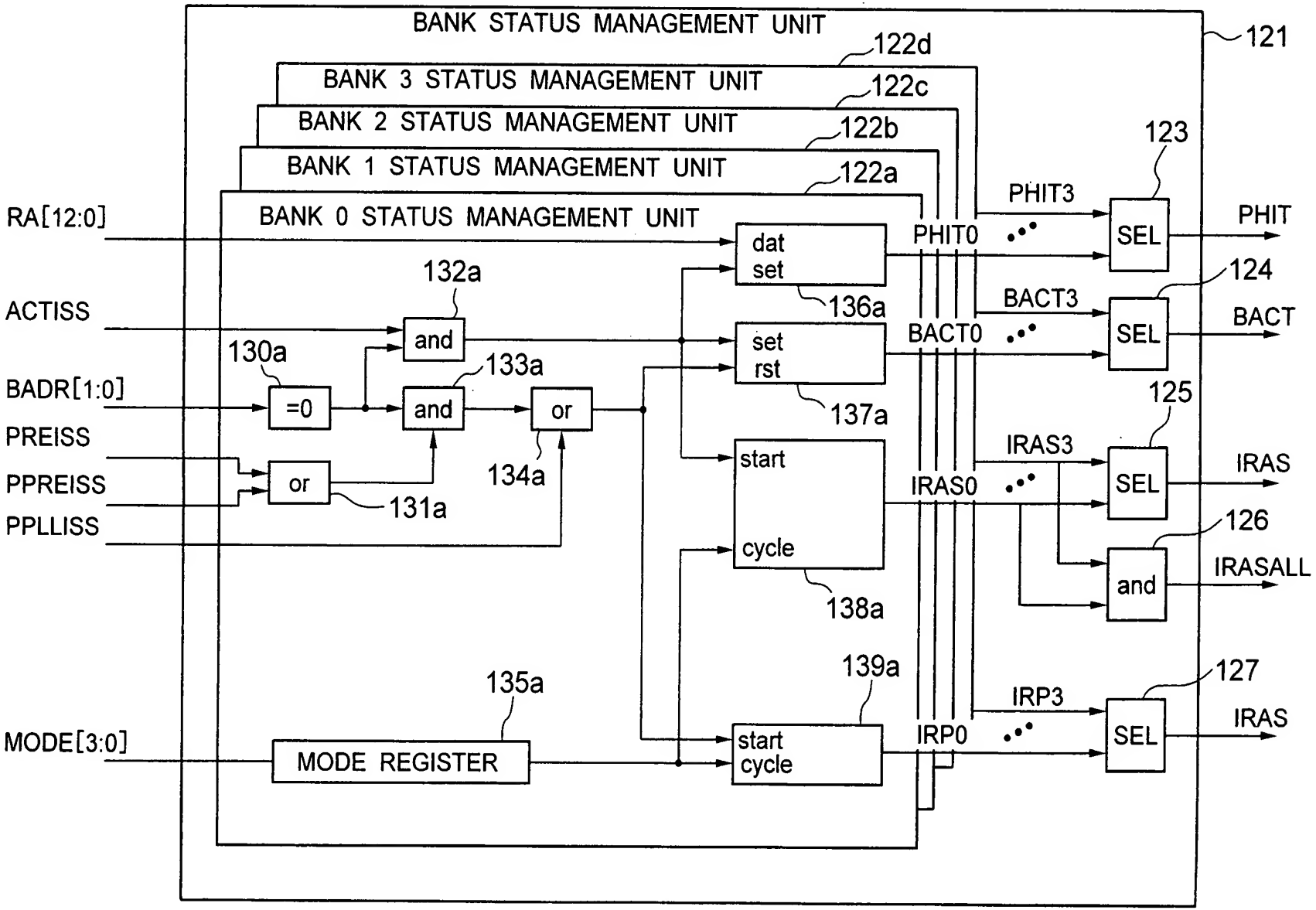

BANK STATUS MANAGEMENT UNIT
121
BANK 3 STATUS MANAGEMENT UNIT
122d
BANK 2 STATUS MANAGEMENT UNIT
122c
BANK 1 STATUS MANAGEMENT UNIT
122b
BANK 0 STATUS MANAGEMENT UNIT
122a
123
RA[12:0]
ACTISS
BADR[1:0]
PREISS
PPREISS
PPLLISS
MODE[3:0]
MODE REGISTER
135a
132a
and
130a
=0
133a
and
or
134a
or
131a
dat
set
136a
set
rst
137a
start
cycle
138a
139a
start
cycle
PHIT3
PHIT0
BACT3
BACT0
IRAS3
IRAS0
IRP3
IRP0
SEL
PHIT
124
SEL
BACT
125
SEL
IRAS
126
and
IRASALL
127
SEL
IRAS

FIG. 14

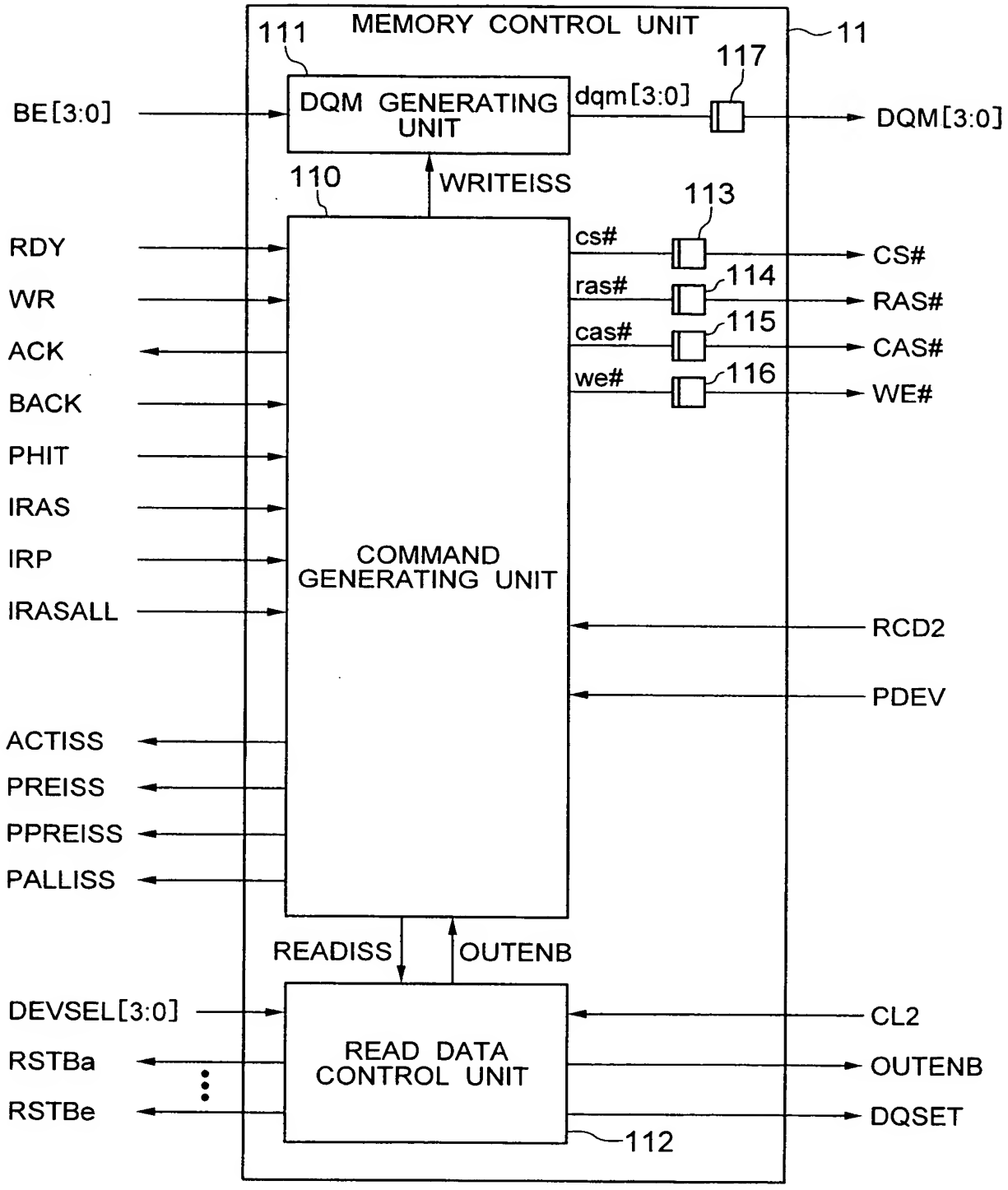

MEMORY CONTROL UNIT
11
111
DQM GENERATING UNIT
117
BE[3:0]
dqm[3:0]
DQM[3:0]
110
WRITEISS
113
RDY
WR
ACK
BACK
PHIT
IRAS
IRP
IRASALL
cs#
ras#
cas#
we#
114
115
116
CS#
RAS#
CAS#
WE#
COMMAND GENERATING UNIT
RCD2
PDEV
ACTISS
PREISS
PPREISS
PALLISS
READISS
OUTENB
DEVSEL[3:0]
RSTBa
RSTBe
READ DATA CONTROL UNIT
CL2
OUTENB
DQSET
112

FIG. 15

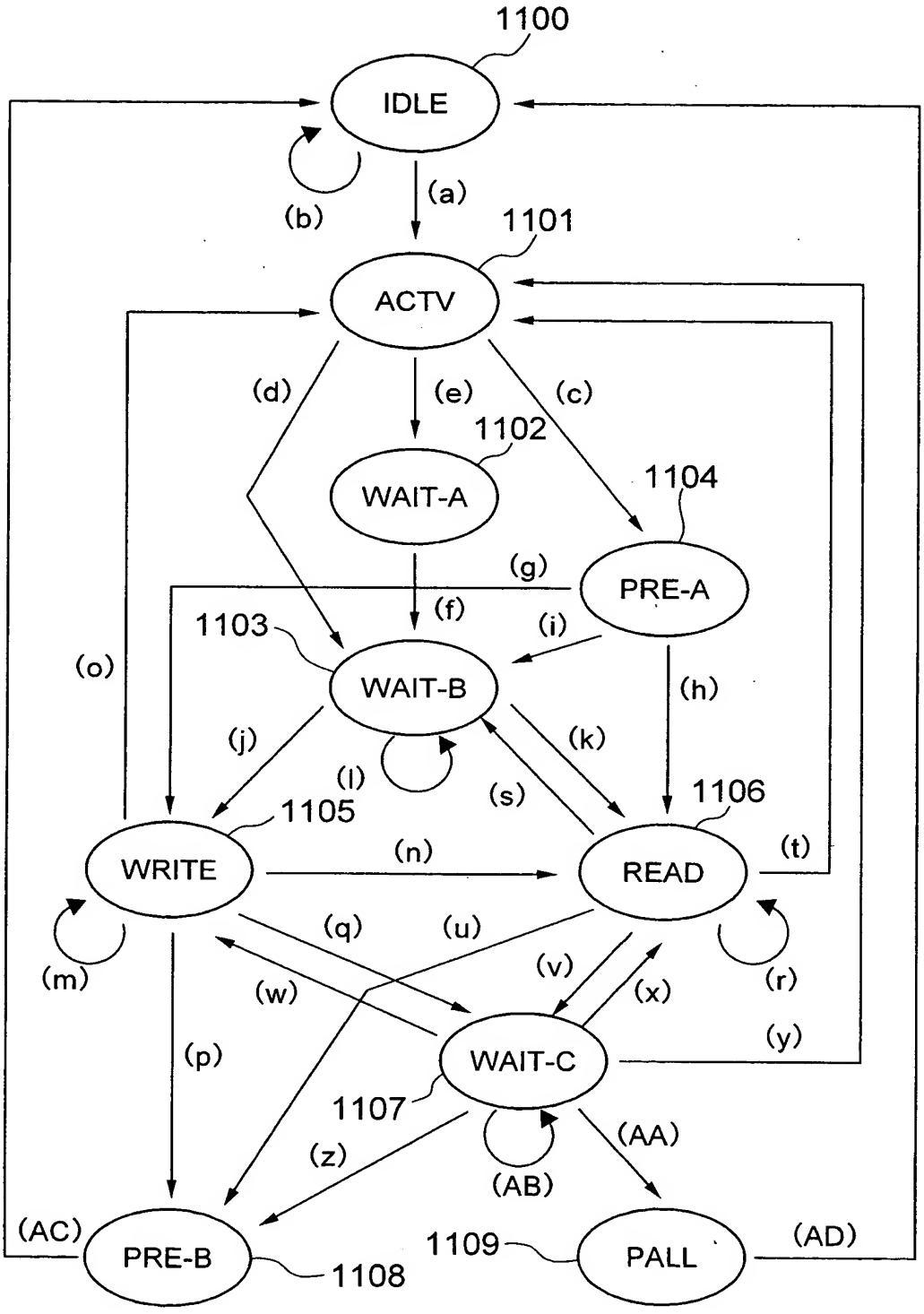

1100
IDLE
(b)
(a)
1101
ACTV
(d)
(e)
(c)
1102
WAIT-A
1104
PRE-A
(g)
(f)
(i)
1103
(o)
WAIT-B
(h)
(j)
(k)
(l)
(s)
1106
1105
WRITE
(n)
READ
(t)
(m)
(q)
(u)
(v)
(x)
(r)
(w)
(y)
(p)
WAIT-C
1107
(z)
(AA)
(AB)
(AC)
PRE-B
1108
1109
PALL
(AD)

FIG. 16

#	TRANSITION SOURCE	TRANSITION DESTINATION	TRANSITION CONDITIONS
a	IDLE	ACTV	RDY & $\overline{\text{IRP}}$
b	IDLE	IDLE	(otherwise)
c	ACTV	PRE-A	PDEV
d	ACTV	WAIT-B	$\overline{\text{PDEV}}$ & RCD2
e	ACTV	WAIT-A	(otherwise)
f	WAIT-A	WAIT-B	(everything)
g	PRE-A	WRITE	CL2 & WR & OUTENB
h	PRE-A	READ	CL2 & $\overline{\text{WR}}$
i	PRE-A	WAIT-B	(otherwise)
j	WAIT-B	WRITE	WR & OUTENB
k	WAIT-B	READ	RDY & $\overline{\text{WR}}$
l	WAIT-B	WAIT-B	(otherwise)
m	WRITE	WRITE	RDY & PHIT & WR
n	WRITE	READ	RDY & PHIT & $\overline{\text{WR}}$
o	WRITE	ACTV	RDY & $\overline{\text{PHIT}}$ & $\overline{\text{BACT}}$ & IRP
p	WRITE	PRE-B	RDY & $\overline{\text{PHIT}}$ & BACT & IRAS
q	WRITE	WAIT-C	(otherwise)
r	READ	READ	RDY & PHIT & $\overline{\text{WR}}$
s	READ	WAIT-B	RDY & PHIT & WR
t	READ	ACTV	RDY & $\overline{\text{PHIT}}$ & $\overline{\text{BACT}}$ & IRP
u	READ	PRE-B	RDY & $\overline{\text{PHIT}}$ & BACT & IRAS
v	READ	WAIT-C	(otherwise)
w	WAIT-C	WRITE	RDY & PHIT & WR & $\overline{\text{OUTENB}}$
x	WAIT-C	READ	RDY & PHIT & $\overline{\text{WR}}$
y	WAIT-C	ACTV	RDY & $\overline{\text{PHIT}}$ & $\overline{\text{BACT}}$ & IRP
z	WAIT-C	PRE-B	RDY & $\overline{\text{PHIT}}$ & BACT & IRAS
AA	WAIT-C	PALL	$\overline{\text{RDY}}$ & IRASALL
AB	WAIT-C	WAIT-C	(otherwise)
AC	PRE-B	IDLE	(everything)
AD	PALL	IDLE	(everything)

FIG. 17

TRANSITION DESTINATION STATUS	OUTPUT SIGNAL										
	ACK	ACTISS	PREISS	PPREISS	PALLISS	WRITEISS	READISS	cs#	ras#	cas#	we#
IDLE	0	0	0	0	0	0	0	1	1	1	1
ACTV	0	1	0	0	0	0	0	0	0	1	1
WAIT-A	0	0	0	0	0	0	0	0	1	1	1
WAIT-B	0	0	0	0	0	0	0	0	1	1	1
PRE-A	0	0	0	1	0	0	0	0	0	1	0
WRITE	1	0	0	0	0	1	0	0	1	0	0
READ	1	0	0	0	0	0	1	0	1	0	1
WAIT-C	0	0	0	0	0	0	0	0	1	1	1
PRE-B	0	0	1	0	0	0	0	0	0	1	0
PALL	0	0	0	0	1	0	0	0	0	1	0

FIG. 18

WRITEISS	OUTPUT SIGNAL			
	DQM3	DQM2	DQM1	DQM0
0	0	0	0	0
1	$\overline{\text{BE}}$[3]	$\overline{\text{BE}}$[2]	$\overline{\text{BE}}$[1]	$\overline{\text{BE}}$[0]

FIG. 19

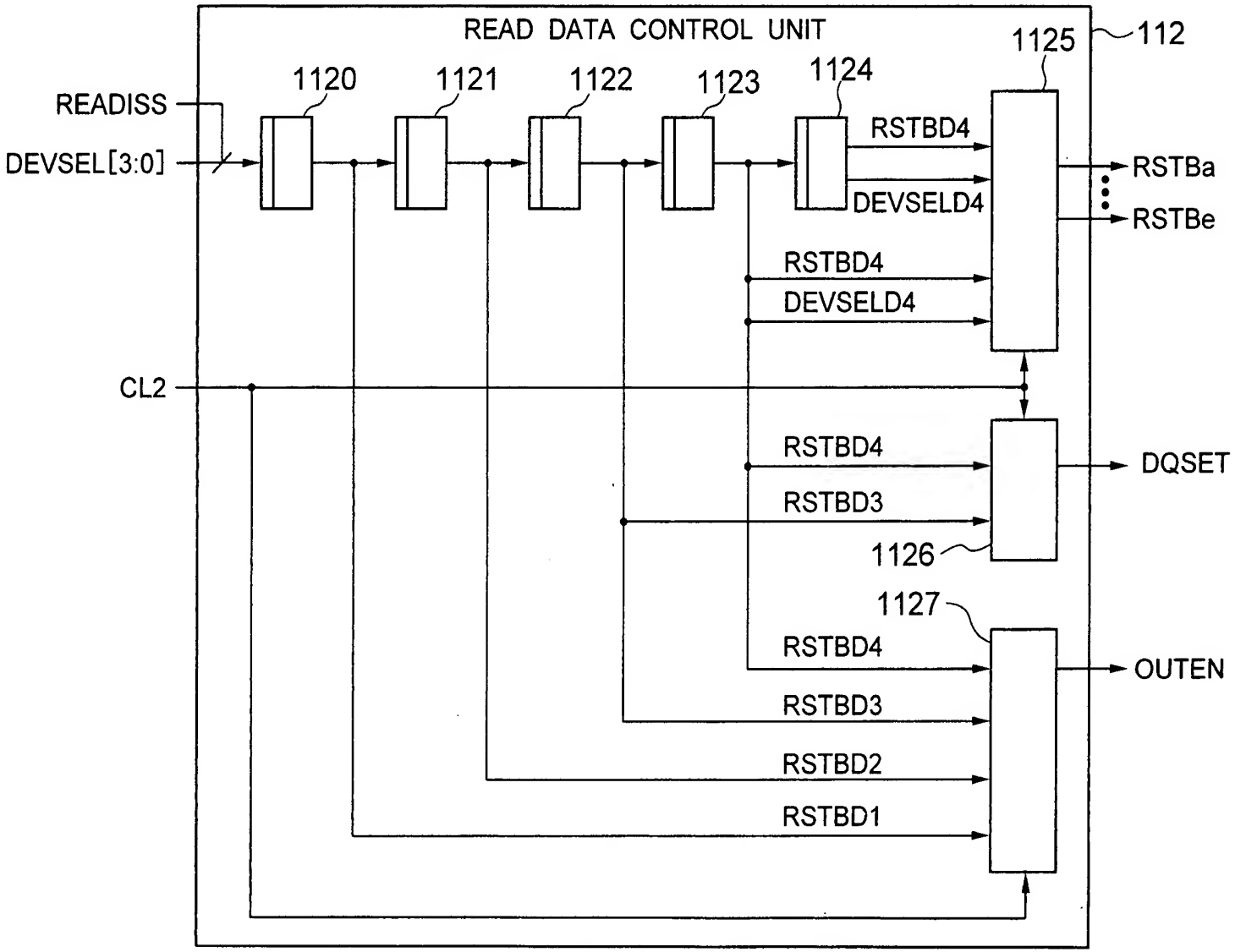

READ DATA CONTROL UNIT
112
1125
1120
1121
1122
1123
1124
READISS
DEVSEL[3:0]
RSTBD4
DEVSELD4
RSTBa
RSTBe
RSTBD4
DEVSELD4
CL2
RSTBD4
RSTBD3
DQSET
1126
1127
RSTBD4
RSTBD3
RSTBD2
RSTBD1
OUTEN

FIG. 20

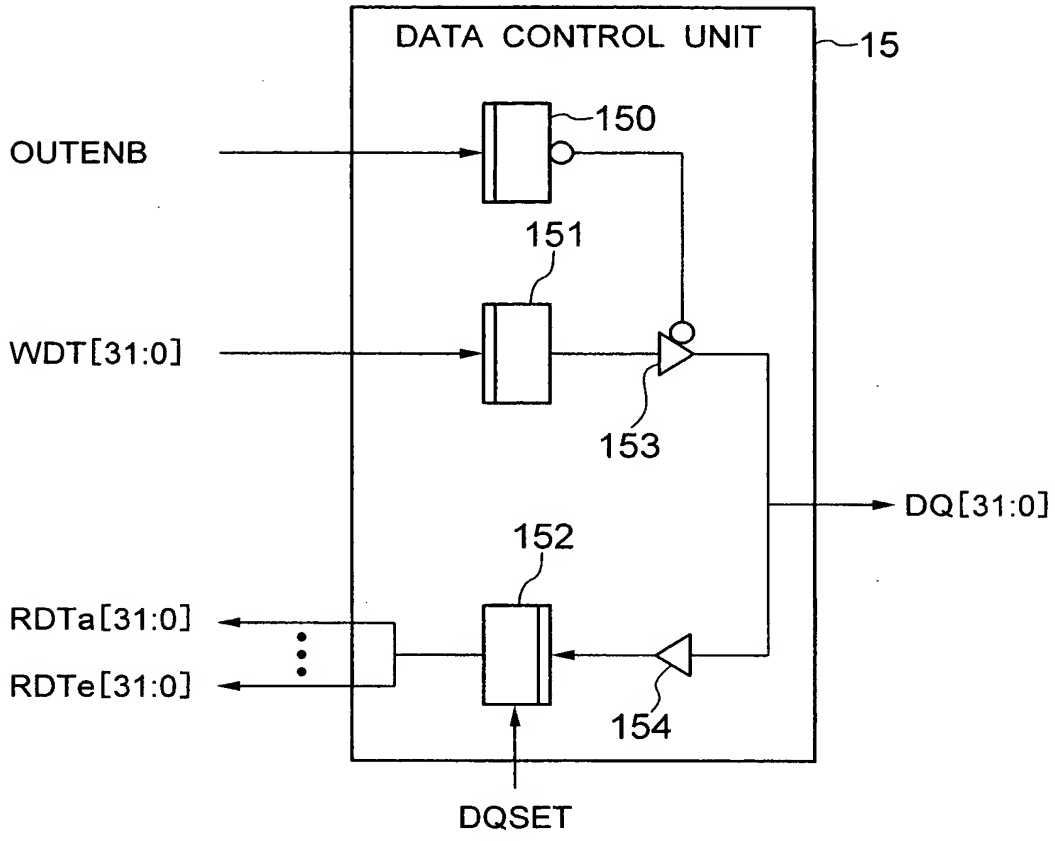

DATA CONTROL UNIT
15
150
OUTENB
151
WDT[31:0]
153
DQ[31:0]
152
RDTa[31:0]
RDTe[31:0]
154
DQSET

FIG. 21

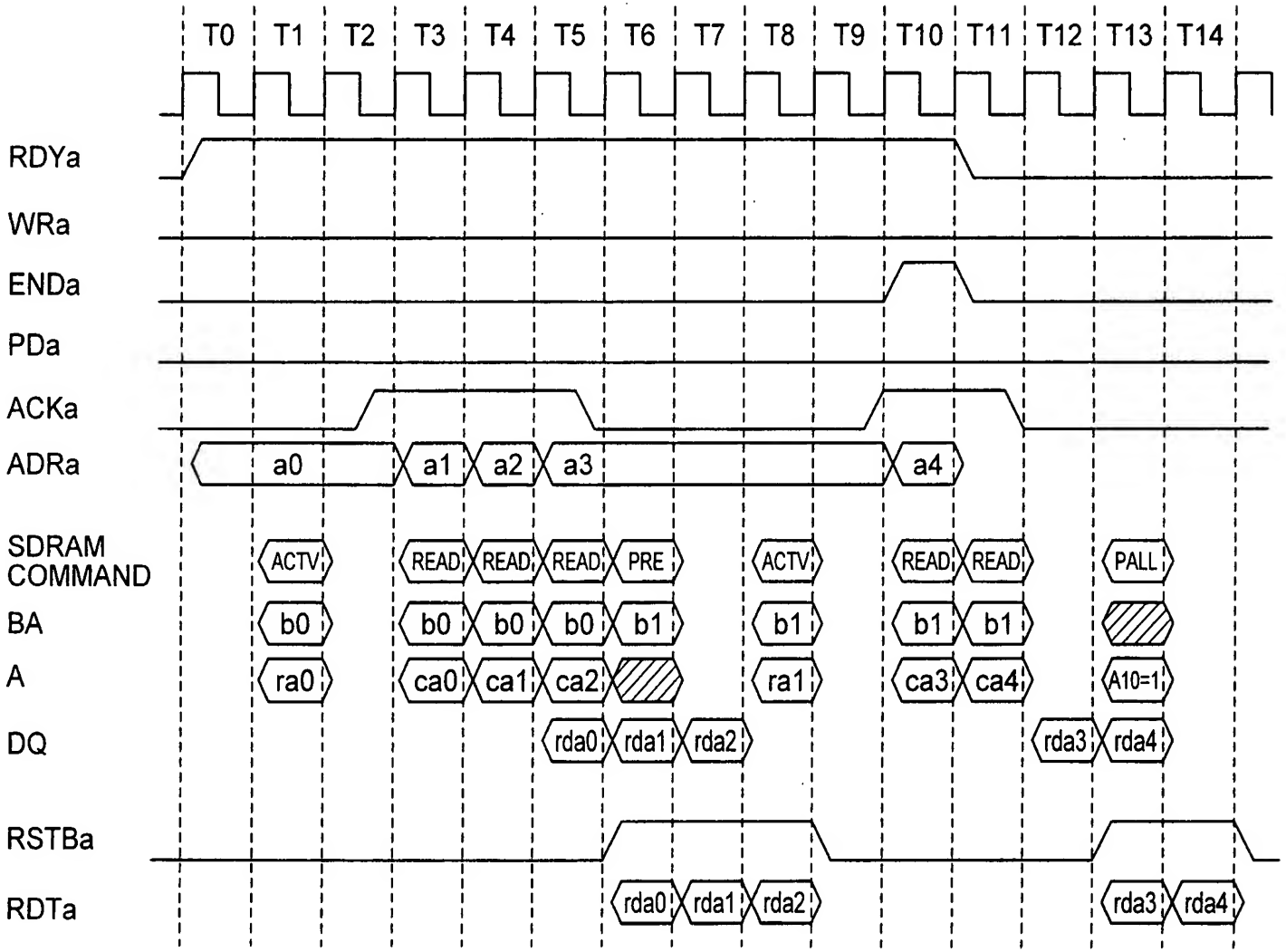
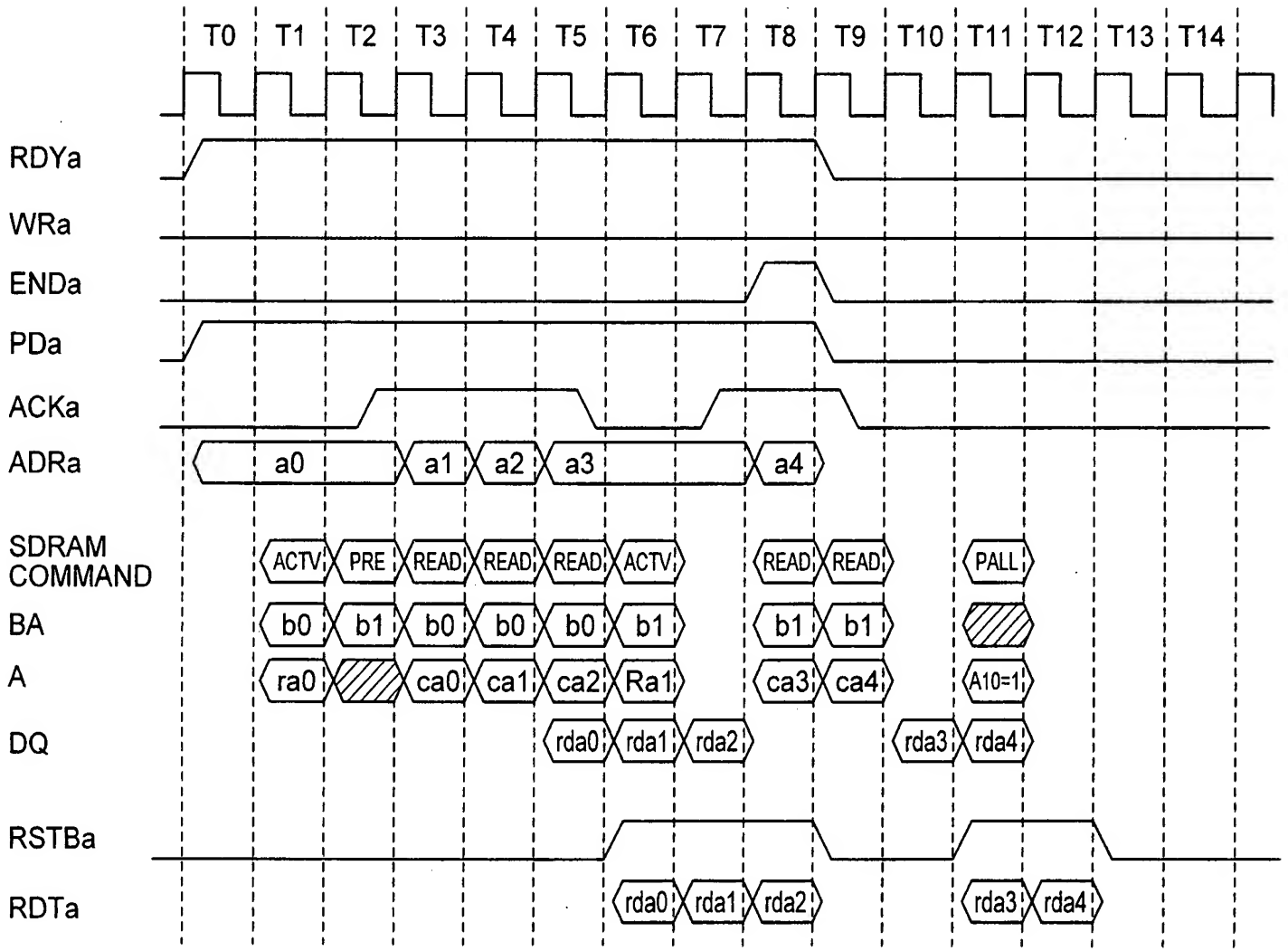

T0
T1
T2
T3
T4
T5
T6
T7
T8
T9
T10
T11
T12
T13
T14
RDYa
WRa
ENDa
PDa
ACKa
ADRa
a0
a1
a2
a3
a4
SDRAM COMMAND
ACTV
READ
READ
READ
PRE
ACTV
READ
READ
PALL
BA
b0
b0
b0
b0
b1
b1
b1
b1
A
ra0
ca0
ca1
ca2
ra1
ca3
ca4
A10=1
DQ
rda0
rda1
rda2
rda3
rda4
RSTBa
RDTa
rda0
rda1
rda2
rda3
rda4

FIG. 22


T0
T1
T2
T3
T4
T5
T6
T7
T8
T9
T10
T11
T12
T13
T14
RDYa
WRa
ENDa
PDa
ACKa
ADRa
a0
a1
a2
a3
a4
SDRAM COMMAND
ACTV
PRE
READ
READ
READ
ACTV
READ
READ
PALL
BA
b0
b1
b0
b0
b0
b1
b1
b1
A
ra0
ca0
ca1
ca2
Ra1
ca3
ca4
A10=1
DQ
rda0
rda1
rda2
rda3
rda4
RSTBa
RDTa
rda0
rda1
rda2
rda3
rda4